1. A digital follower device comprising:

an n-channel vertical FET device; and

a p-channel vertical FET device wherein each said vertical FET device comprises:

a bulk region in a semiconductor substrate wherein said bulk region comprises a first doping type;

a STI region in said bulk region;

a drain region on a first side of said STI region wherein said drain region overlies said bulk region and wherein said drain region comprises said first doping type;

a gate region on a second side of said STI region wherein said gate region comprises said first doping type and wherein a voltage on said gate region controls a vertical channel in said bulk region; and

a buried region between said gate region and said bulk region wherein said buried region comprises a second doping type, wherein said n-channel FET device drain and said p-channel FET device drain are coupled together, and wherein said n-channel FET device gate and said p-channel FET device gate are connected together.

2. The device according to Claim 1 wherein said p-channel

FET device bulk region comprises said semiconductor substrate and wherein said n-channel FET device bulk comprises an n-well region in said semiconductor substrate.

3. The device according to Claim 1 wherein said n-channel FET device gate region comprises an n+ region and said n-channel FET device buried region comprises a p+ region.

4. The device according to Claim 1 wherein said p-channel FET device gate region comprises an p+ region and said p-channel FET device buried region comprises a n+ region.

5. The device according to Claim 1 wherein an additional STI region is formed in said semiconductor substrate, wherein trenches for said vertical FET device STI regions and said additional STI region are formed simultaneously, and wherein said vertical FET device STI regions comprise a lower dielectric constant than the dielectric constant of said additional STI region.

6. The device according to Claim 1 wherein both said gates and both said drains are further connected together to form a storage node of a latch device.

7. The device according to Claim 6 further comprising a switch to controllably connect said storage node and a bit line.

8. A digital latch device comprising:

an n-channel vertical FET device; and

a p-channel vertical FET device wherein each said vertical FET device comprises:

a bulk region in a semiconductor substrate wherein said bulk region comprises a first doping type;

a STI region in said bulk region;

a drain region on a first side of said STI region wherein said drain region overlies said bulk region and wherein said drain region comprises said first doping type;

a gate region on a second side of said STI region wherein said gate region comprises said first doping type and wherein a voltage on said gate region controls a vertical channel in said bulk region; and

a buried region between said gate region and said bulk region wherein said buried region comprises a second doping type, wherein said n-channel FET device drain and gate and said p-channel FET device drain and

gate are connected together to form a storage node for said digital latch device.

9. The device according to Claim 8 wherein said p-channel FET device bulk region comprises said semiconductor substrate and wherein said n-channel FET device bulk comprises an n-well region in said semiconductor substrate.

10. The device according to Claim 8 wherein said n-channel FET device gate region comprises an n+ region and said n-channel FET device buried region comprises a p+ region.

11. The device according to Claim 8 wherein said p-channel FET device gate region comprises an p+ region and said p-channel FET device buried region comprises a n+ region.

12. The device according to Claim 8 wherein an additional STI region is formed in said semiconductor substrate, wherein trenches for said vertical FET device STI regions and said additional STI region are formed simultaneously, and wherein said vertical FET device STI regions comprise a lower dielectric constant than the dielectric constant of said additional STI region.

13. The device according to Claim 8 further comprising a switch to controllably connect said storage node and a bit line.

14. The device according to Claim 13 wherein said switch comprises a MOSFET.

15. An SRAM cell device comprising:

a digital latch comprising:

an n-channel vertical FET device; and

a p-channel vertical FET device wherein each said vertical FET device comprises:

a bulk region in a semiconductor substrate wherein said bulk region comprises a first doping type;

a STI region in said bulk region;

a drain region on a first side of said STI region wherein said drain region overlies said bulk region and wherein said drain region comprises said first doping type;

a gate region on a second side of said STI region wherein said gate region comprises said first doping type and wherein a voltage on said

gate region controls a vertical channel in said bulk region; and

a buried region between said gate region and said bulk region wherein said buried region comprises a second doping type, wherein said n-channel FET device drain and gate and said p-channel FET device drain and gate are connected together to form a storage node for said digital latch device; and

a switch to controllably connect ~~couple~~ said storage node and a bit line.

16. The device according to Claim 15 wherein said p-channel FET device bulk region comprises said semiconductor substrate and wherein said n-channel FET device bulk region comprises an n-well region in said semiconductor substrate.

17. The device according to Claim 15 wherein said n-channel FET device gate region comprises an n+ region and said n-channel FET device buried region comprises a p+ region.

18. The device according to Claim 15 wherein said p-

channel FET device gate region comprises an p+ region and said p-channel FET device buried region comprises a n+ region.

19. The device according to Claim 15 wherein an additional STI region is formed in said semiconductor substrate, wherein trenches for said vertical FET device STI regions and said additional STI region are formed simultaneously, and wherein said vertical FET device STI regions comprise a lower dielectric constant than the dielectric constant of said additional STI region.

20. The device according to Claim 15 wherein said switch comprises a MOSFET.

21. A SRAM cell device comprising:

a first digital latch; and

a second digital latch wherein said first and second digital latches each comprise an n-channel vertical FET device and a p-channel vertical FET device and wherein each said vertical FET device comprises:

a bulk region in a semiconductor substrate wherein said bulk region comprises a first doping type;

a STI region in said bulk region;

a drain region on a first side of said STI region wherein said drain region overlies said bulk region and wherein said drain region comprises said first doping type;

a gate region on a second side of said STI region wherein said gate region comprises said first doping type and wherein a voltage on said gate region controls a vertical channel in said bulk region; and

a buried region between said gate region and said bulk region wherein said buried region comprises a second doping type, wherein said n-channel FET device drain and gate and said p-channel FET device drain and gate are connected together to form a storage node for said digital latch device; and

a switch to controllably connect said storage node and a bit line.

22. The device according to Claim 21 wherein said p-channel FET device bulk region comprises said semiconductor substrate and wherein said n-channel FET device bulk region comprises an n-well region in said semiconductor substrate.

23. The device according to Claim 21 wherein said n-channel

FET device gate region comprises an n+ region and said n-channel FET device buried region comprises a p+ region.

24. The device according to Claim 21 wherein said p-channel FET device gate region comprises an p+ region and said p-channel FET device buried region comprises a n+ region.

25. The device according to Claim 21 wherein an additional STI region is formed in said semiconductor substrate, wherein trenches for said vertical FET device STI regions and said additional STI region are formed simultaneously, and wherein said vertical FET device STI regions comprises a lower dielectric constant than the dielectric constant of said additional STI region.

26. The device according to Claim 21 wherein said switch comprises a MOSFET.

27. The device according to Claim 21 wherein said first digital latch switch and said second digital latch switch are controlled by a single word line for said SRAM cell device.

28. A method to form digital follower devices each comprising an n-channel vertical FET and a p-channel vertical FET device, said method comprising:

forming n-channel vertical FET devices and p-channel vertical FET devices wherein said vertical FET devices are formed by a method comprising:

forming STI regions in a semiconductor substrate;

forming bulk regions of a first doping type in said semiconductor substrate;

implanting ions into said bulk regions on a first side of said STI regions to thereby form drain regions wherein said drain regions comprise said first doping type and wherein said drain regions overlie said bulk regions;

implanting ions into said bulk regions on a second side of said STI regions to form gate regions wherein said gate regions comprise said first doping type and wherein voltages on said gate regions control vertical channels in said bulk regions; and

implanting ions into said bulk regions on said second side of said STI regions to form buried regions between said gate regions and said bulk regions wherein said buried regions comprise a second doping type; and

forming connective lines to connect together said n-channel FET device drain regions and said p-channel FET device drain regions and to connect together said n-channel FET device gate regions and said p-channel FET device gate regions.

29. The method according to Claim 28 wherein said p-channel FET device bulk regions comprises said semiconductor substrate and wherein said n-channel FET device bulk regions comprises an n-well region in said semiconductor substrate.

30. The method according to Claim 28 wherein said n-channel FET device gate regions comprises an n+ region and said n-channel FET device buried regions comprises a p+ region.

31. The method according to Claim 28 wherein said p-channel FET device gate regions comprise a p+ region and said p-channel FET device buried regions comprise a n+ region.

32. The method according to Claim 28 wherein said step of forming STI regions comprises:

etching trenches in said semiconductor substrate for said STI regions and for other STI regions;

selectively filling said trenches for said STI regions with a first dielectric layer and said trenches for said other STI regions with a second dielectric layer wherein said first dielectric layer comprises a lower dielectric constant than said second dielectric layer; and

planarizing said first and second dielectric layers to complete said STI regions and said other STI regions.

33. The method according to Claim 28 wherein both said drain regions and both said gate regions are connected together to form a storage node.

34. The method according to Claim 33 further comprising:

depositing a polysilicon gate layer overlying said semiconductor substrate; and

patterning said polysilicon layer to form gates for MOSFET devices wherein said MOSFET devices comprise switches to controllably connect said storage node and a bit line.